REMARKS

Claims 1-6 are pending.

The Office action objected to the use of the phrase "adapted to" in the claims stating that such a phrase is not a limiting phrase. Applicant notes that various decisions by the Court of Appeals for the Federal Circuit suggest that use of the phrase "adapted to . . ." in the body of a claim may serve as a substantive limitation. *See, e.g., Ishida Co. v. Taylor*, 55 USPQ2d 1449, 1453 (Fed. Cir.2000) (interpreting the phrase "a pair of sealing and stripping means . . . being adapted to cooperate . . ."); *Intermatic Inc. v. Lamson & Sessions Co.*, 61 USPQ2d 1075, 1983 (Fed. Cir. 2001). Nevertheless, the word "adapted" has been deleted from the claims. Therefore, applicant respectfully requests withdrawal of the objections.

The claims were rejected over the prior art as follows:

* Claims 1 and 4 were rejected as unpatentable over the combination of U.S. Patent Nos. 4,639,919 (Chang et al.) and 4,876,685 (Rich).

* Claims 2, 3, 5 and 6 were rejected as unpatentable over the combination of the Chang et al. and Rich patents in view of U.S. Patent No. 6,587,983 (Nakayama).

Claims 1 and 4 have been amended to recite that "when the operation mode is in a first state, the data log is acquired from a limited range of test pattern addresses so as to include an address at which a FAIL signal is generated, and when the operation mode is in a second state, the data log is acquired for all test pattern addresses in the range." *See, e.g.*, page 15, lines 10-12 and page 18, lines 16-19 of the pending specification.

Thus, the present application claims a log memory that stores the address of the executed test pattern. The data log acquisition includes generation of the write address where a "Fail" signal occurred, and the address of a test pattern. The state of the mode generator determines which range of addresses is stored in the log memory.

The Chang et al. patent discloses a pattern generator where each pin 20 of a device-under-test (DUT) 18 receives an input sequence through a respective driver/receiver 22. The Chang et al. device has a plurality of pattern generators 24, one for each DUT pin 20. Each pin pattern generator generates its own bit sequence for the respective DUT pin. A 256-bit collective output from the shift registers 96 provides a single 256-bit input word to an error flag log memory 102. The 256-bit collective output is stored in the error flag log memory 102 at an address determined by the output from a memory address register 110. However, the Chang et al. reference does not disclose that an address of a test pattern is stored and that there is more than one storage technique depending on the state of a mode generator.

The Rich reference a memory tester for processing failure information of a memory under test. The device includes a pattern generator 12 that provides XY addresses 22, and data from a data generator 23 to a DUT 14. A random access memory 16 stores failure information related to the DUT. However, the Rich reference also does not disclose a mode generator having multiple states where the particular state alters the range of addresses stored in the log memory.

The Nakayama patent does not disclose or suggest the features missing from the other references.

In view of the foregoing amendments and remarks, applicant respectfully requests reconsideration and withdrawal of the rejections of the claims.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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